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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,245	10/22/2003	Hemant G. Rotithor	P16243	8373

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EXAMINER	
SCHLIE, PAUL W	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,245	ROTITHOR ET AL.	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-70 have been examined.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-70 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure that is not enabling. Sufficiently comprehensive detailed structural logic and timing diagrams, and concise algorithmic descriptions detailing corresponding structural implementation if so envisioned are considered critical or essential to the practice of the invention, but not included in the claims and not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

As for example within claim 1, although a method is claimed comprising "sorting memory transactions into at least one queue" by their attributes, no such corresponding detailed structural or corresponding logical procedural description is disclosed in sufficient detail which would enable one of ordinary skill in the art to functionally replicate this disclosed element of the invention without likely substantial effort and/or experimentation, although presumably a critical element of the claimed invention. All rejected claims lack similar corresponding critical element and/or inter-element implementation details.

The applicant is reminded that no new subject matter may be introduced beyond that which is currently present within the disclosure. Corrective action is required.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

5. Claims 7, 36 and 46 are rejected, as the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 4-5, 30-31, 33-34, 42, 44, 37-38 and 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (5,948,081) in further view of Jenne et al. (US App. Pub. No. 2002/0065981).

As per claims 1, 30, 37-38 and 47-48, Foster teaches a method and/or apparatus embodying a method for out-of-order memory (inclusive of multi-bank DRAM) transaction scheduling comprising: sorting memory transactions into at least one queue by source transaction and/or target memory attributes and/or state, such that the effective transactions and their corresponding memory commands are more ideally sequenced so as to optimize memory command interface efficiency and/or critical transaction latency (see Foster figure 3, column 3-4 lines 45-7), however does not explicitly teach that such scheduling selection may occur at the time of command launch. Jenne teaches that such a selection may be made at the time of command

launch by explicitly depicting the queued commands which may result from the most current optimal schedule which may be selected at command launch (see figure 8). It would be obvious to one of ordinary skill in the art to combine the two, to enable the most recently received transaction request to potentially effect the optimal scheduling of commands up-to the time of command launch, for the benefit of optimizing memory command interface efficiency and/or critical transaction latency.

As per claims 2, 31 and 42 being dependent on claim 1, 30, or 37 respectively, Foster further teaches that a queue may be allowed to fill up without delaying memory (DRAM) command being issued (see figure 3). Therefore it would be obvious to one of ordinary skill in the art to allow a queue to fill up without delaying a memory (DRAM) command, as command selection is clearly only naturally delayed by the absents of presently queued transaction requests, not their increasing presence. It would be obvious to one of ordinary skill in the art to allow a queue to fill up without delaying a memory (DRAM) command, for the benefit of not introducing likely otherwise counterproductive transaction latency.

As per claims 4-5, 33-34 and 44 being dependant on claim 1, 30 or 37 respectively, Jenne et al. further teaches that a previously otherwise selected write command sequence may be preempted by a read command to optimize read latency; and thereby may potentially increase command interval timing associated with the previously initiated command sequence, and/or command sequences which have been interleaved to optimize aggregate command efficiency. (see figure 10, element 304). It would be obvious to one of ordinary skill in the art to recognize these effects may

factually result from a more optimal scheduling of command sequences to achieve more optimal command efficiency and/or critical transaction latency.

8. Claims 3, 32, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (5,948,081) and Jenne et al. (US App. Pub. No. 2002/0065981) in further view of Wulf et al. (6,154,826).

As per claim 3, 32 and 43, being dependent on claim 1, 30 or 37 respectively, but neither Foster nor Jenne et al. teach that commands may be prioritized without regard to the presently active page. Wulf et al. further teaches that commands may be scheduled without regard to the memory's current page state (see column 29, lines 22-25). It would be obvious to one of ordinary skill in the art to combine enable a schedule to disregard a memory page's present hit state, for the potential benefit of simplifying an implementation.

9. Claims 6-29, 35-36, 39-41, 45-46 and 49-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (5,948,081) and Jenne et al. (US App. Pub. No. 2002/0065981), in further view of Saracovsky et al. (6,378,049).

As per claims 6, 35 and 45 being dependent on claim 1, 30 or 37 respectively, but neither Foster nor Jenne et al. teach explicitly that multiple components (ranks) or banks may have corresponding physical queues. Saracovsky et al. teaches that memory may be comprised of multiple components (ranks) which may be comprised of multiple components and may be hierarchically arranged, thereby enabling individual memory controllers to be associated with individual ranks if so desired, thereby enabling physically distinct queues to be associated with each (see column 12-13, lines 61-3). It

is considered obvious to one of ordinary skill in the art to provide a potentially distinct queue for each rank and/or bank (where further multiple physical queues for banks within each rank may be considered logically equivalent to a single queue, as any set of M element x N queues who's elements are collectively treated as an aggregate is logically equivalent to an single NxM element queue, see Jenne et al. column 7 lines 9-13), for the benefit of enabling command sequences to individual ranks to be processed in parallel with respect to each other.

As per claims 7, 36 and 46 being dependent on claim 1, 30 or 37 respectively, but neither Foster or Jenne et al. teach that transactions may be sorted including attributes "such as" (which is considered to be indefinite limitation, see above), address mappings, priority, etc. transaction types. However Saracovsky et al. does teach that processor priority may also be considered for transaction prioritization (see column 5 lines 8-12). It would be obvious to one of ordinary skill in the art to enable transactions to be sorted as a function of any attribute considered to be significant to the performance goals of an implementation, for the benefit of achieving those goals.

As per claims 8-29 and 39-41 being dependant on claim 1, 30 or 37, and potentially subsequent dependant claims inclusively; Foster further teaches that the number of consecutive otherwise prioritized read requests to the same, and/or potentially different pages, may be limited so that potentially older pending requests (including the oldest pending write to the currently active page, or globally oldest pending transaction) may be given an opportunity to be serviced without potentially aging indefinitely (see column 3 lines 18-20); regardless of the number of physical

queues, as multiple physical queues subject as an aggregate subject to a given selection/sorting criteria are considered equivalent to a single queue subject to the same criteria (see Jenne et al. column 7 lines 9-13). It would be obvious to one of ordinary skill in the art to combine this knowledge to potentially limit the number of sequential prioritized transactions of any particular type which may be embodied in any number of physically distinct queues, for the benefit of enabling potentially lesser priority transactions to be periodically serviced, thereby effectively limiting their worst case latencies, thereby also lessening the likelihood of any particular type of transaction from dominating the pending queued transactions, which may otherwise compromise an implementation's ability to derive a reasonably optimal schedule. Where further it would be obvious to one of ordinary skill in the art to utilize conventionally utilized logic elements inclusive of comparators, and/or correspondingly more complex logic structures such as arbitrators and/or associative memories, etc., to implement correspondingly desired logical behaviors as may be embodied within a digital microelectronic based apparatus.

As per claims 49-70, where 49 being independent, and remaining dependant on claim 49, 58, 62, 65 or 68, and potentially subsequent dependant claims inclusively; Foster further teaches that the number of consecutive otherwise prioritized read requests to the same, and/or potentially different pages, may be limited so that potentially older pending requests (including the oldest pending write to the currently active page, or globally oldest pending transaction) may be given an opportunity to be serviced without potentially aging indefinitely (see column 3 lines 18-20); regardless of

the number of physical queues, as multiple physical queues subject as an aggregate subject to a given selection/sorting criteria are considered equivalent to a single queue subject to the same criteria (see Jenne et al. column 7 lines 9-13). It would be obvious to one of ordinary skill in the art to combine this knowledge to potentially limit the number of sequential prioritized transactions of any particular type which may be embodied in any number of physically distinct queues, for the benefit of enabling potentially lesser priority transactions to be periodically serviced, thereby effectively limiting their worst case latencies, thereby also lessening the likelihood of any particular type of transaction from dominating the pending queued transactions, which may otherwise compromise an implementation's ability to derive a reasonably optimal schedule. Where further it would be obvious to one of ordinary skill in the art to utilize conventionally utilized logic elements inclusive of comparators, and/or correspondingly more complex logic structures such as arbitrators and/or associative memories, etc., to implement correspondingly desired logical behaviors as may be embodied within a digital microelectronic based apparatus.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER